REMARKS

Claims 1-40, all the claims pending in the application, stand rejected on prior art grounds. Claims 18-19 and 33 are objected to. Claims 1-8, 14-22 and 36-40 stand rejected upon informalities. Claims 1-8 and 36-40 stand rejected under 35 U.S.C. §101. Applicants respectfully traverse these rejections based on the following discussion.

I. Claim Interpretation

The Office Action interprets the language of claim 1 as follows:

Claim 1: "the first bounded range of the performance parameter is understood as process parameters associated to a process model for individual manufacturing process executed on a CAD system. Similarly, the second bounded range of the performance parameter is understood as device parameters associated to a device model executed on a CAD system."

The Applicants traverse this interpretation and amend claim 1 to clarify the meaning of the first and second bounded ranges. Specifically, as amended, claim 1 refers to "a simulator comprising a computer model of an integrated circuit device having at least one performance attribute, wherein said computer model comprises a target performance parameter for said performance attribute." A first bounded range for this target performance parameter comprises "performance parameter variations within a single manufacturing process based on a single design for said device," and a second bounded range for this target performance parameter comprises performance parameter variations between multiple designs for said device." See paragraphs [0004], [0018], [0022], [0028], [0034], and [0047] and Figure 2. The first bounded range does not refer to "process parameters", but rather to a target performance parameter value that may vary within this first bounded range based on the manufacturing process variations

which may be present when the device is manufactured according a given design. The second bounded range on the other hand does not refer to "device parameters" (e.g., line width or other such device parameters), but again to the same target performance parameter value that varies within this second bounded range based on variations in between different designs.

In view of the foregoing, the Examiner is respectfully requested to reconsider the interpretation of the claim language.

II. Claim Objections

Claims 18, 19 and 33 were objected to under 37 C.F.R. 1.75(c) and have been amended to overcome the objections.

III. Rejections of Claims 1-8 under 35 U.S.C. §112, ¶1

Claims 1-8 were rejected under 35 U.S.C. §112, ¶1, as failing to comply with the enablement requirement. The Applicants respectfully traverse these rejections because the Examiner has not established a prima facie case supporting why independent claim 1 and its dependent claims 2-8 are not adequately enabled by the description of the invention provided in the specification (see In re Wright, 999 F.2d 157, 27 USPQ 2d 1510, 1513 (Fed. Cir. 1993)). Specifically, the Office Action rejects independent claim 1 (and, consequently, dependent claims 2-8) under 35 U.S.C. §112, ¶1 because "as recited the claim does not enable any one to make/design a computer model of a device just be describing the performance parameters of the device." However, 35 U.S.C. §112, ¶1 provides that the "specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best

mode contemplated by the inventor of carrying out his invention." Thus, 35 U.S.C. §112, ¶1 rejections should address not what the claim, as written, enables but rather whether or not the features of the claimed invention are enabled by the specification.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. Rejection of Claims 14-22, and 36-40 under 35 U.S.C. §112, ¶2

A. Rejection of Independent Claim 14.

Independent claim 14 provides "a method of developing a product having a device" and, particularly, claims the steps used to develop the product. As amended, the claimed steps include providing design goals, developing a target performance parameter, producing a target model based on the design goals and the target performance parameter, and designing the product and the device based on the model. This claim was rejected under 35 U.S.C. §112, ¶2 because, the Office Action asserts, the terms developing, product, device, and target model are subject to various interpretations. More specifically, the Office Action narrowly interpreted the word "developing" as conceptual representation of the actual device (not a real manufactured device) and then asserted that the claim does not provide any difference between the product, device and target model. The Applicants traverse this rejection.

When rejecting a claim under 35 U.S.C. §112, ¶2, the "[d]efiniteness of claim language is analyzed, not in a vacuum, but always in light of the teachings of the prior art and of the particular application disclosure as it would be interpreted by one possessing the ordinary level of skill in the pertinent art." (see In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971). See

also MPEP 2173.02). Furthermore, "The definiteness of claim language must also be analyzed in light of the claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. W. L. Gore & Assoc., Inc. v. Garlock, Inc., 220 USPQ 303 (Fed. Cir. 1983). Therefore, contrary to the Examiner's decisions, the Applicants respectfully assert that if the claim language were analyzed based on both the teachings of the prior art and on the information disclosed in the present application, it would be considered by one with an ordinary skill in the art to be definite.

More specifically, the Applicants assert that the word "developing" was unambiguous and should not have been so narrowly interpreted "as conceptual representation of the actual device (not a real manufactured device.)" The plain and ordinary meaning of the term "developing" in the context of "developing a product" clearly refers to making something new, namely the product (see *WordNet ® 2.0, © 2003 Princeton University*). Figure 4 details the process flow through production. Thus, the features of claim 14 refer to how a product is made (e.g., providing goals, developing a target performance parameter, producing a target model, designing the device, etc.). While the claim does not include the final step of manufacturing the product based on the design, it doesn't have to because this final step is not the novel feature of the invention.

Furthermore, the Applicants assert that the distinction between the product and the device is clear and that it is explained in detail in paragraph [0017] of the specification. Paragraph [0017] indicates that in "the preferred embodiment, "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. However, it is

to be understood that the invention is also applicable to any component of any product, where the performance attributes of that component help determine the functionality of the integrated product. Examples include chemical components and subcomponents of a drug, or the insole of a shoe, or the foam insulation of a hot tub. In each example, the former is the "device" and the latter is the "product"." Furthermore, what is claimed in claim 14 is a method of "developing a product having a device." The plain and ordinary meaning of the term "having" in this context clearly refers to possessing or containing as a constituent part (see *The American Heritage® Dictionary of the English Language, Fourth EditionCopyright © 2000 by Houghton Mifflin Company.Published by Houghton Mifflin Company.*) Thus, the device referred to in claim 14 is to be a constituent part of the product being developed by the method of claim 14.

The Applicants also assert that the distinction between the device and the target model is clear. That is, as mentioned in paragraph [0002], product development necessitates design tools such as computer models. In the method "[T]here are a number of different individuals or different teams that are involved in the design/manufacture of a final product. For example, when designing integrated circuits, a process designer is responsible for designing and manufacturing specific implants or dielectric layers. A device designer (e.g., transistor developer) uses the components designed/manufactured by the process developer to create individual devices (transistors). A circuit designer utilizes the different devices designed/manufactured by the transistor developer to create complete integrated circuits." See paragraph [0023]. Paragraph [0032] further explains that in the development processes "[D]evice goals are established and that "the device goals are merely conceptual objectives that the device should achieve, and do not represent a true model of the device. From these goals, the

target performance parameters 404 are developed." Then, based on the target performance parameters a target model is produced (see paragraph [0034]). Target or compact models are a set of equations that are typically embodied in a set of physics-based software subroutines that are part of a circuit network simulation program (see paragraphs [0004] and [0047]). The actual designs for the device as well as the designs for the overall product are also produced based on the target performance parameters (see paragraphs [0034-37]). Thus, steps that are used in the claim 14 method of developing a product having a device include both producing a target model of the device and also designing the device.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection as well as the rejection of dependent claims 15-18.

B. Rejection of Independent Claim 19.

Claim 19 is amended herein to eliminate any issues of indefiniteness. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection as well as the rejection of dependent claims 20-22.

C. Rejection of Independent Claims 36 and 40.

The Office Action rejects claims 36 and 40 asserting that there is insufficient antecedent basis for the limitation "computer medium." However, the "computer medium" is the subject matter of the claim, not a claim limitation that requires an antecedent basis. Furthermore, support for this feature is found in paragraph [0049] which provides that "[a] program storage device readable by the disk or tape units, is used to load the instructions which operate on a compact modeling system which is also loaded onto the computer system." In view of the

foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 36 and 40 as well as the rejection of dependent claims 37-39.

V. Rejection of Claims 1-8 and 36-40 under 35 U.S.C. §101

Claims 1-8, and 36-40 stand rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Independent claims 1, 36 and 40 are amended herein to overcome the rejections under 35 U.S.C. §101. More specifically, paragraphs [0004] and [0047] of the specification disclose that the computer model of the invention comprises physics-based subroutines used in numerical simulation codes and, more particularly, that the target model is a set of equations (typically embodied in a set of software subroutines that are part of a circuit network simulation program). Paragraph [0049] further discloses a representative hardware environment for practicing the present invention.

Consequently, claim 1 is amended herein to overcome the 35 U.S.C. §101 rejection by claiming not the computer model alone, but rather the simulator in which the computer model is embodied. Claims 36 and 40 are amended herein to overcome the 35 U.S.C. §101 rejection by claiming computer mediums storing "a computer model of an integrated circuit device having at least one performance attribute, said model comprising a set of subroutines created using a target performance parameter for said performance attribute" and "designs for an integrated circuit device having at least one performance attribute, wherein said designs are generated utilizing a computer model, said model comprising a set of subroutines created using a target performance parameter for said performance attribute," respectively.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

VI. Rejection of Claims 1-40 under 35 U.S.C. §103(a)

Claims 1-27, and 30-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al. (U.S. Patent No. 6,269,277) hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic. Applicants respectfully traverse these rejections based on the following discussion. Claims 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, in view of Krivokapic, in further view of Peng, et al. (U.S. Patent No. 6,028,994), hereinafter referred to as Peng.

A. Rejection of Independent claims 1, 9, 14, 19, 24, 36 and 40.

Regarding independent claims 1, 9, 14, 19, 24, 36 and 40 the Applicants submit that neither Hershenson, nor Krivokapic teach or suggest the feature that "said target performance parameter includes a first bounded range and a second bounded range, wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and wherein said second bounded range comprises performance parameter variations between multiple designs for said device."

The Office Action cites col. 4, Lines 5-26 of Hershenson as disclosing a "performance parameter includes a first bounded range and a second bounded range as inequality constraints." The Applicants respectfully disagree. More specifically, the Applicant's submit that Hershenson does not teach that the performance parameter includes two different bounded ranges, but rather teaches how to optimize a selected performance parameter.

The cited portions of Hershenson provide that a user selects a performance specification for a desired device and that this performance specification is described as a posynomial function of a design parameter (see col. 3, line 67-col. 4, line 2). Those skilled in the art will recognize that a posynomial function is not a bounded range, but rather are a positive sum of monomials. Such posynomials are fundamental functions in geometric programming. Performance specifications combined with user defined design objectives and constraints are combined to form a geometric program (see col. 4, lines 2-5 and col. 5, line 62-col. 6, line 2). These programs are reformulated as optimization problems (see col. 4, lines 5-6). That is, the performance specifications are optimized subject to a set of constraints or subject to a set of constraints and several process conditions (see col. 6, lines 1-24). Thus, a performance specification in Hershenson is selected and defined as a function of the design process and then optimized based on constraints and/or processing conditions in order to provide a globally optimal performance specification (see col. 6, lines 20-24). Thus, the performance specification in Hershenson is not defined in terms of bounded ranges but rather an optimal value and, particularly, not in terms of a first bounded range that comprises performance parameter variations within a single manufacturing process for a single design for a device and a second bounded range that comprises performance parameter variations between multiple designs for a device.

The Office Action further admits that Hershenson does not teach that the first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for the device. Thus, the Office Action cites Figure 6a-6b, the Abstract, col. 19-27 and col. 8, lines 50-63 of Krivokapic as teaching this feature. Specifically, the Office

Action indicates that Krivokapic teaches "a semiconductor process simulator"... "and process parameters for individual processes"... "are sampled in and or simulated from the Monte Carlo Engine..." The Office Action further indicates that Krivokapic teaches range bounds. However, these are not features of the claimed invention. That is, independent claims 1 and 36 each claim a set of equations that is created using "a target performance parameter" for a specific "performance attribute" of an integrated circuit device. The target performance parameter has two different bounded ranges: a first bounded range that comprises performance parameter variations within a single manufacturing process based on a single design for the device and a second bounded range that comprises performance parameter variations between multiple designs for the device. Thus, these ranges refer to the variations in the performance parameter of the performance attribute of the device once it is manufactured, whether the variations are the result of manufacturing variations or actual design variations. Neither of these bounded ranges refer to the different processing parameters for the various different processes that are used to manufacture the device.

Therefore, independent claims 1, 9, 14, 19, 24, 36 and 40 are patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 2-8, 9-13, 15-18, 20-22, 25-35 and 37-39 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection of independent claim 19.

In additional to the features described above with regard to claim 19, the cited prior art also does not teach or suggest the following features: (1) "proposing a modification of the design that comprises either adding a particular feature into the design or modifying an already present feature; and (2) "balancing design choices related to said modification and, particularly, to said primary parameters and said secondary parameters so that said target performance parameter remains within said first bounded range and said second bounded range."

Specifically, the cited portions of Krivokapic teach a method in which a simulator is run on semiconductors having primary attributes in order to determine curves for secondary attributes and, thereby, to obtain worst-case curves for the secondary attributes. Parameters are then extracted from the worst-case curves in order to determine accurate worst-case semiconductor designs. Contrarily, the present invention determines the primary parameters associated with a particular feature to be modified in a design and then determines which secondary parameters will be affected by these primary parameters. Then, design choices related to the modification and, particularly, related to the primary and secondary parameters are balanced to achieve some goal, yet still maintain the target performance parameter within the established ranges (see paragraph [0044]).

Therefore, independent claim 19 is further patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 20-22 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

C. Rejection of independent claim 23.

The Office Action indicates that claim 23 discloses similar limitations as claim 1 and that it is rejected for the same reasons as claim 1. More specifically, citing Hershenson col. 5, line 63- col. 6, line 24, the Office Action indicates that Hershenson teaches each of the following features of claim 23: (1) "determining a set of design distributions that are within a given set of performance targets for a plurality of parameters;" (2) "altering different features of said design; and" (3) "determining whether said altered design is within said set of design distributions." The Applicants respectfully traverse this rejection.

As mentioned above, Hershenson provides a method in which a user selects a performance specification for a desired device and this selected performance specification is described as a posynomial function of a design parameter (see col. 3, line 67-col. 4, line 2). Those skilled in the art will recognize that a posynomial function is not a bounded range, but rather are a positive sum of monomials. Such posynomials are fundamental functions in geometric programming. Performance specifications combined with user defined design objectives and constraints are combined to form a geometric program (see col. 4, lines 2-5 and col. 5, line 62-col. 6, line 2). These programs are reformulated as optimization problems (see col. 4, lines 5-6). That is, the performance specifications are optimized subject to a set of constraints or subject to a set of constraints and several process conditions (see col. 6, lines 1-24). Thus, a performance specification in Hershenson is selected and defined as a function of the design process and then optimized based on constraints and/or processing conditions in order to provide a globally optimal performance specification (see col. 6, lines 20-24).

Thus, the performance specification in Hershenson is not defined in terms of a set of design distributions to allow for varying designs or varying processes for a single design, but rather an optimal value to be applied globally. Furthermore, Hershenson does not address altering different features of the design, nor does it address altering different features of the design and then determining whether the altered design is within the set of design distributions.

Therefore, independent claim 23 is further patentable over Hershenson in combination with Krivokapic. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.